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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

SWICKHAMER, CHRISTOPHER M

ART UNIT	PAPER NUMBER
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2697

DATE MAILED: 01/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/452,751

Applicant(s)

FIELD ET AL.

Examiner

Christopher M Swickhamer

Art Unit

2697

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 January 2000.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 December 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 & 6. 6) ☐ Other: _____

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements filed 8/30/02 and 11/21/02 fail to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. Please submit documents G-T from the IDS received 8/30/02.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "52" in Fig. 2 and "50" on page 12, line 3 have both been used to designate "Internal Interface". This list is not inclusive. All reference characters within the specification and drawings must agree. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to under 37 CFR 1.83(a) because they fail to show details of how the "switch core" is connected to the "switch slots" and "line slots" as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 7-12, and 14-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Colmant (US Patent No. 5,953,330). Referring to Claim 1, Colmant discloses a synchronous switch for a telecommunications node, comprising: a switch interface unit (SIU, switch interface) operable to terminate a bus and to receive a time division multiplexed frame from the bus (a frame having a plurality of time slots, Fig. 1, col. 4, lns. 52-64, col. 5, lns. 36-40) that are each operable to transport a packet (traffic cell, col. 4, lns. 50-55); a controller (switch controller) operable to determine a type for each packet (traffic cell) received at the SIU (switch interface) and to determine based on the type for a packet (traffic cell) the appropriate queue for the cell (col. 6, lns. 35-44), such as a synchronous or asynchronous cell (an address for storing the traffic cell in a switch memory); and the FDDI RAM Buffer (FRB, switch memory) operable to receive the packet (traffic cell) from the SIU (switch interface) and the appropriate queue information

(address) for storing the packet (traffic cell) from the controller (switch controller) and to store the packet (traffic cell) in the queue (at the address, col. 7, lns. 30-52).

- Referring to Claim 2, Colmant discloses the synchronous switch of Claim 1, further comprising: the Packet and Media Access Control (P-MAC, switch interface) operable to extract a header for the traffic cell from a time division multiplexed packet (time slot transporting the traffic cell, col. 7, lns. 30-52) and to provide the header to the controller (switch controller); and the queue manager in the controller (switch controller) further operable to determine the type for the packet (traffic cell) based on the header (col. 7, lns. 30-52).

- Referring to Claim 3, Colmant discloses the synchronous switch of Claim 1, further comprising: the switch memory comprising a plurality of synchronous queues (time division multiplex, TDM, memory slots) and a plurality of asynchronous queues (asynchronous transfer mode, ATM) associated with output ports (col. 7, lns. 30-52); and the controller (switch controller) further operable to determine an address of an asynchronous (ATM) queue in the FRB (switch memory) for storing a packet (traffic cell) in response to determining the packet (traffic cell) is asynchronous (ATM type) and to determine a queue (an address) for a synchronous packet (TDM memory slot) in the FRB (switch memory) for storing a packet (traffic cell) in response to determining the packet is synchronous (traffic cell is of a TDM type, Fig. 5, col. 7, lns. 30-52).

- Referring to Claim 4, Colmant discloses the synchronous switch of Claim 3, further comprising: the P-MAC (switch interface) operable to extract a header for the packet (traffic cell) from a time slot transporting the packet (traffic cell) and to provide the header to the queue manager in the controller (switch controller); and the queue manager (switch controller) further

Art Unit: 2697

operable to determine whether the packet (traffic cell) is asynchronous (of the ATM type) or synchronous (the TDM type) based on the header (col. 7, lns. 30-52).

- Referring to Claim 5, Colmant discloses the synchronous switch of Claim 1, wherein the SIU (switch interface), controller (switch controller), and FRB (switch memory) each operate at a speed to handle an 80 ns byte stream (synchronized frame pulse, col. 4, lns. 50-64).

- Referring to Claim 7, Colmant discloses the synchronous switch of Claim 1, further comprising the SIU (switch interface) operable to terminate a plurality of point-to-point links of the bus and to receive from each link a frame having a plurality of the time slots. A bus inherently meets this limitation since a bus is an electrical connection that allows two or more wires or lines to be connected together.

- Referring to Claim 8, Colmant discloses the synchronous switch of Claim 7, wherein the point-to-point links of the bus operate at disparate rates. ATM supports traffic which has different priorities to support traffic of different rates, such as constant bit rate (CBR), variable bit rate, (VBR, col. 14, lns. 49-56).

- Referring to Claim 9, Colmant discloses the synchronous switch of Claim 1, wherein the packet (traffic cell) comprises an ATM cell (col. 14, lns. 49-57).

- Referring to Claim 10, Colmant discloses the synchronous switch of Claim 1, further comprising: the SIU (switch interface) further operable to transmit on the bus a time division multiplexed packet stream (an egress frame comprising a plurality of egress time slots) that are operable to transport a packet (traffic cell, col. 5, lns. 15-45); the controller (switch controller) further operable to determine an address in the FRB (switch) memory storing a packet (traffic cell) for transport in a time division multiplexed packet stream (an egress time slot) and to

Art Unit: 2697

provide the address to the FRB (switch memory, col. 5, lns. 5, lns. 40-60); and the FRB (switch memory) operable to write the packet (traffic cell) at the address in the FRB (switch memory) to the time division multiplexed packet (the egress time slot) for transmission on the bus (col. 5, lns. 30-col. 6, lns. 13).

- Referring to Claim 11, Colmant discloses a adapter (switch card) for a telecommunications node, comprising: a SIU (switch interface) operable to terminate a bus (plurality of point-to-point links) with data operating at disparate rates, such as ATM which allows for different rates (Fig. 1, col. 14, lns. 49-56), to receive from each link a frame a time division multiplexed packet (having a plurality of time slots) that are each operable to transport a packet (traffic cell, col. 5, lns. 30-50), a P-MAC to extract a header for a packet (traffic cell) from the time slot transporting the packet (traffic cell), and to provide the header to a controller (switch controller, col. 7, lns. 30-52); the controller (switch controller) operable to determine a type for the packet (traffic cell) based on the header, to determine based on the type an address for storing the packet (traffic cell) in a FRB (switch memory, col. 7, lns. 30-52), and to provide the address to the FRB (switch memory); and the FRB (switch memory) operable to receive the packet (traffic cell) from the SIU (switch interface) and the address for storing the packet (traffic cell) from the controller (switch controller), to associate the address with the packet (traffic cell), and to store the packet (traffic cell) at the address (col. 7, lns. 30-52).

- Referring to Claim 12, Colmant discloses the adapter (switch card) of Claim 11, wherein the SIU (switch interface), controller (switch controller), and FRB (switch memory) each operate at a synchronized frame pulse (col. 4, lns. 50-64).

- Referring to Claim 14, Colmant discloses the adapter (switch card) of Claim 11, further comprising: the SIU (switch interface) further operable to transmit on the bus (each of the point-to-point links) a time division multiplexed packet (an egress frame comprising a plurality of egress time slots) that are each operable to transport a packet (traffic cell, col. 5, lns. 15-col. 6, lns 13); the controller (switch controller) further operable to determine an address in the FRB (switch memory) storing a packet (traffic cell) to be transported in an egress time slot on a point-to-point link and to provide the address to the FRB (switch memory, col. 5, lns. 50-col. 6, lns 13); and the FRB (switch memory) operable to write the packet (traffic cell) at the address in the FRB (switch memory) to the egress time slot for transmission on the bus (point-to-point link, col. 5, lns. 30-45).

- Referring to Claim 15, Colmant discloses a method for switching traffic at a telecommunications node, comprising: receiving a frame comprising a plurality of time slots each having a packet (traffic cell) and a header for the packet (traffic cell, col. 5, lns. 30-45); determining a type for each packet (traffic cell) based on the header for the packet (traffic cell); determining an address in the FRB (switch memory) for storing the packet (traffic cell) based on the type and storing the packet (traffic cell) in the FRB (switch memory) at the address (col. 7, lns. 30-52).

- Referring to Claim 16, Colmant discloses the method of Claim 15, further comprising: receiving the frame at a SIU (switch interface); extracting the header from the time slots at the SIU (switch interface); passing the headers to a controller (switch controller); and determining the address at the controller (switch controller) based on the header (col. 7, lns. 30-52).

- Referring to Claim 17, Colmant discloses the method of Claim 16, further comprising:
passing the packet (traffic cell) from the SIU (switch interface) to the FRB (switch memory);
passing the address from the controller (switch controller) to the FRB (switch memory); and
associating the address with the packet (traffic cell) at the FRB (switch memory, Fig. 4A, col. 7, lns. 1-52).

- Referring to Claim 18, Colmant discloses the method of Claim 17, further comprising
operating the SIU (switch interface), controller (switch controller), and FRB (switch memory) at
a synchronized frame pulse (col. 4, lns. 50-64, col. 7, lns. 20-30).

- Referring to Claim 19, Colmant discloses the method of Claim 15, wherein the FRB
(switch memory) comprises a synchronous queue (plurality of time division multiplex, TDM,
memory slots) and an asynchronous queue (plurality of asynchronous transfer mode, ATM,
queues) associated with output ports, further comprising determining an address of an
asynchronous (ATM) queue in the FRB (switch memory) for storing a packet (traffic cell) in
response to determining the traffic cell is of an ATM type (col. 7, lns. 30-52).

- Referring to Claim 20, Colmant discloses the method of Claim 19, further comprising
determining an address of a synchronous queue (TDM memory slot) in the FRB (switch
memory) for storing a packet (traffic cell) in response to determining the packet (traffic cell) is
synchronous (of a TDM type, col. 7, lns 30-52).

- Referring to Claim 21, Colmant discloses the method of Claim 15, further comprising
receiving a time division multiplexed frame from the bus (each of a plurality of point-to-point
links of a bus, each frame comprising a plurality of the time slots, col. 5, lns. 30-50).

- Referring to Claim 22, Colmant discloses the method of Claim 15, further comprising: transmitting a time division multiplexed packet (an egress frame comprising a plurality of egress time slots) that are each operable to transport a packet (traffic cell); determining an address in the FRB (switch memory) storing a packet (traffic cell) for transport in an egress time slot; and writing the traffic cell at the address in the FRB (switch memory) to the egress time slot for transmission in the egress frame (col. 5, lns. 15-col. 6, lns. 12).

- Referring to Claim 23, Colmant discloses the method of Claim 16, further comprising: the SIU (switch interface) transmitting a time division multiplexed packet (an egress frame comprising a plurality of egress time slots) that are each operable to transport a packet (traffic cell); the controller (switch controller) determining an address in the FRB (switch memory) storing a packet (traffic cell) for transport in an egress time slot and providing the address to the FRB (switch memory); and the FRB (switch memory) writing the packet (traffic cell) at the address in the FRB (switch memory) to the egress time slot for transmission in the egress frame (col. 5, lns. 15-col. 6, lns. 12).

- Referring to Claim 24, Colmant discloses the system for switching traffic at telecommunications node, comprising: a computer-readable medium; and software stored on the computer-readable medium (col. 7, lns. 30-52), the software operable to receive a frame comprising of a time division multiplexed packet (plurality of time slots) each having a packet (traffic cell) and a header for the packet (traffic cell), to determine a type for each packet (traffic cell) based on the header for the packet (traffic cell), to determine an address in a FRB (switch memory) for storing the packet (traffic cell) based on the type, and to store the packet (traffic cell) in the FRB (switch memory) at the address (col. 7, lns. 30-52).

- Referring to Claim 25, Colmant discloses the system of Claim 24, the software comprising a SIU (switch interface) and a controller (switch controller), the software further operable to receive the frame at the SIU (switch interface), the P-MAC to extract the header from the time slots at the SIU (switch interface), to pass the header to the controller (switch controller), and to determine the address at the controller (switch controller) based on the header (col. 7, lns. 30-52).

- Referring to Claim 26, Colmant discloses the system of Claim 25, the software further operable to pass a packet (traffic cell) from the SIU (switch interface) to the FRB (switch memory), to pass the address from the controller (switch controller) to the FRB (switch memory), and to associate the address with the packet (traffic cell) at the FRB (switch memory, col. 7, lns. 30-52).

- Referring to Claim 27, Colmant discloses the system of Claim 26, the software further operable to operate the SIU (switch interface), controller (switch controller), and FRB (switch memory) at a synchronized frame pulse (col. 4, lns. 50-64, col. 7, lns. 20-30).

- Referring to Claim 28, Colmant discloses the system of Claim 24, wherein the FRB (switch memory) comprises a synchronous queue (plurality of time division multiplex, TDM, memory slots) and a asynchronous queue (plurality of asynchronous transfer mode, ATM, queues) associated with output ports, the software further operable to determine an address of an asynchronous (ATM) queue in the FRB (switch memory) for storing a packet (traffic cell) in response to determining the packet (traffic cell) is asynchronous (of an ATM type, col. 7, lns. 30-52, col. 14, lns. 49-56).

- Referring to Claim 29, Colmant discloses the system of Claim 28, the software further operable to determine an address of a synchronous queue (TDM memory slot) in the FRB (switch memory) for storing a packet (traffic cell) in response to determining the packet (traffic cell) is synchronous (of a TDM type, col. 7, lns. 30-52).

- Referring to Claim 30, Colmant discloses the system of Claim 24, the software further operable to receive a frame from the bus (each of a plurality of point-to-point links of a bus), each frame is time division multiplexed (comprising a plurality of time slots, col. 5, lns. 30-50).

- Referring to Claim 31, Colmant discloses the system of Claim 24, the software further operable to transmit an egress frame comprising a plurality of egress time slots that are each operable to transport a packet (traffic cell), to determine an address in the FRB (switch memory) storing a packet (traffic cell) for transport in an egress time slot, and to write the packet (traffic cell) at the address in the FRB (switch memory) to the egress time slot for transmission in the egress frame (col. 7, lns. 30-52).

- Referring to Claim 32, Colmant discloses the system of Claim 25, the software comprising: the SIU (switch interface) operable to transmit an egress frame comprising a time division multiplexed packet (plurality of egress time slots that) operable to transport a packet (traffic cell); the controller (switch controller) operable to determine an address in the FRB (switch memory) storing a packet (traffic cell) for transport in an egress time slot and to provide the address to the FRB (switch memory); and the FRB (switch memory) operable to write the packet (traffic cell) at the address in the FRB (switch memory) to the egress time slot for transmission in the egress frame (Fig. 4A, col. 7, lns. 30-52, col. 5, lns. 30-50).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colmann in view of Lewis (US Patent No. 6,005,865). Referring to Claim 6, Colmant discloses the synchronous switch of Claim 5, but does not disclose the synchronized frame pulse is a 125 microsecond frame pulse. Lewis discloses a system where the synchronized frame pulse is a 125 microsecond frame pulse (col. 7, lns. 55-60). At the time the invention was made, it would have been obvious to one of ordinary skill to use a 125 microsecond frame pulse size for the frame size used in transmitting the synchronous and asynchronous packet data. One of ordinary skill in the art would have been motivated to do this since 125 microseconds is a standard frame size for time division multiplexed traffic.

- Referring to Claim 13, Colmant discloses the adapter (switch card) of Claim 12, but does not expressly disclose the frame pulse comprises a 125 microsecond frame pulse. Lewis discloses a system where the synchronized frame pulse is a 125 microsecond frame pulse (col. 7, lns. 55-60). At the time the invention was made, it would have been obvious to one of ordinary skill to use a 125 microsecond frame pulse size for the frame size used in transmitting the synchronous and asynchronous packet data. One of ordinary skill in the art would have been motivated to do this since 125 microseconds is a standard frame size for time division multiplexed traffic (col. 7, lns. 30-67).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Hershey et al, US Patent No. 6,167,062. *System and associated method for the synchronization and control of multiplexed payloads over a telecommunications network.*
- Irwin et al, US Patent No. 5,841,771. *Telecommunications switch apparatus and method for time switching.*
- Closs et al, US Patent No. 4,862,451. *Method and apparatus for switching information between channels for synchronous information traffic and asynchronous data packets.*
- Canniff et al, US Patent No. 5,953,330. *Communication Switch.*
- Santore et al, US Patent No. 5,615,211. *Time division multiplexed backplane with packet mode capability.*
- Aimoto, US PG-PUB 2002/0181484 A1. *Packet switch and switching method for switching variable length packets.*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher M Swickhamer whose telephone number is (703) 306.4820. The examiner can normally be reached on 8:00-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (703) 305.4798. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308.9571 for regular communications and (703) 827.9314 for After Final communications.

Art Unit: 2697

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305.3900.

CMS

January 15, 2003


RICKY NGO
PRIMARY EXAMINER